The Design and Testing Challenges of High Voltage RF Circuits

Mark G. Walden
Electromagnetics and RFICs Technology Centre
Roke Manor Research Ltd
Romsey, United Kingdom
mark.walden@roke.co.uk

***Abstract*—The design and testing challenges of High Voltage RF circuits are discussed with particular reference to a recent Solid State Power Amplifier design. Using a single Si MOSFET device, we were able to produce over 2kW of pulsed power at VHF frequencies.**

Keywords-High Voltage; Solid State Power Amplfier; Design; Test;High Voltage Test Chamber

I. INTRODUCTION

High Voltage (HV) Testing Laboratories tend to be university or government run establishments. The few commercial facilities that do exist are typically set up for power generation and distribution component testing. For the Radio Frequency (RF) engineer this can present real problems when testing their HV designs. In this paper I shall discuss the challenges that the RF engineer faces when designing and testing HV RF circuits. For the purposes of this paper I shall base this on the recent development of a HV VHF Solid State Power Amplifier (SSPA).

II. HV SSPA REQUIREMENT AND DEVICE TECHNOLOGY CHOICE

The HV SSPA requirement was for a low cost, compact device delivering around 2kW pulsed power at 150MHz. Further requirements were for very short pulses and very low duty cycle (roughly 100µs pulse length and 0.1% duty cycle).

The first issue to be addressed was the choice of device technology. Several device technologies were considered for this application. Traditional RF communication technologies such as GaAs MESFET and Silicon LDMOS were rejected due to their low supply voltage and their high cost. SiC was also considered, but again the cost was considered too high and the technology not sufficiently mature at this stage. Silicon MOSFET technology emerged as the device technology that would best meet the requirements, with supply voltages of several hundred volts possible, and devices available for reasonable cost.

Power MOSFETs have been used successfully for HF power amplification. Their low cost and ready availability make power MOSFETs ideally suited for applications in the 100's of kiloHertz region. Some have reported their use up to 30MHz [1]. Initially we considered using power MOSFET but found that they have three major drawbacks;

1. high input capacitances – leading to low switching speed
2. device integration (having drain connected to heat sink)
3. packaging - long leads leading to high inductances

Some effort has been made by certain device manufacturers to address some of these problems, but very rarely were all three issues addressed in the same device.

III. MODELLING SI MOSFET DEVICES

It was found that modelling the various Si MOSFET devices with RF and Microwave simulation tools was not straight forward. Device models supplied by the manufacturers were either unhelpful or non existent. Some SPICE modelling was performed, but again with limited success. Often the best approach was to develop a figure of merit for comparison of the candidate devices using such characteristics as input and output capacitances, and to use this to calculate the charge movement that would be required to operate the devices in the VHF region. Often this would give as good an indication as any as to whether a device would be suitable.

IV. TOPOLOGY

We had decided upon a push-pull configuration. This presents its own challenges for the device selection. Unless "mirror image" devices are available, the layout of the amplifier will be compromised. An alternative is to use a device that consists of two die in a single package. Microsemi offers such a device in the ARF475FL [2].

Microsemi also offer a reference design for the ARF475FL at 128MHz [3]. Using this as a starting point Roke designed an amplifier more fitting for our purpose. Several changes to the reference design were enabled. The design was tweaked to increase give the best performance at 150MHz. Our requirement was for fast, short pulses, at low duty cycle. We reasoned that the gate and drain bias circuitry described in the technical note would not support this. Furthermore we wished to control the device such that it was not active during the "off" period. We would use a limited charge storage arrangement to provide the DC bias, and turning the device off would give time for the capacitors used to recharge before the next burst was required. Usually

978-1-61284-079-6/11/$26.00 ©2011 Crown

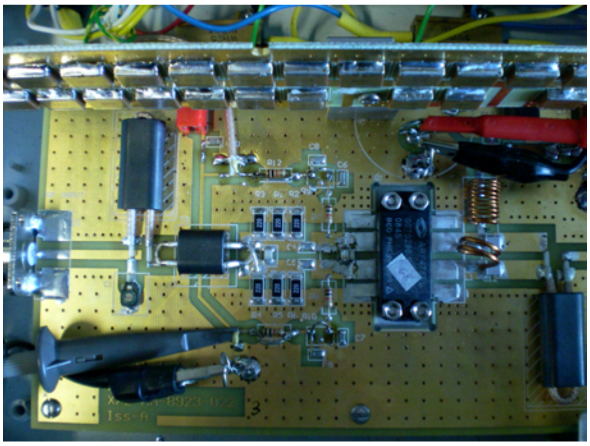

Figure 1. The high power high voltage solid state amplifier.

we would use high side switching to control the device, but in this case, with drain voltages of over 150V present we decided to control the device by use of the gate bias to achieve pinch off. The ARF475FL is pinched off at 0V, but to be sure we arranged for the gate bias to be made negative during the off period.

The control pulse was provided by a PIC microcontroller, programmed to give various length pulses and PRIs, controlled by DIP switches. The output of this was buffered using open collector and fed to a driver MOSFET. This was arranged such that in the off period the device output -5V and during the on pulse it output the gate bias as set by a PSU. Local charge storage and RF decoupling of the drain supply line was provided by AVXs high voltage MLC chip capacitors with X7R dielectric. Bulk storage capacitance was provided by AVX FFVE series polyester capacitors.

For testing purposes the amplifier was placed inside an interlocked safety box. This also contained the charging/discharging circuitry for the storage capacitors, and limited the available energy to safe levels. Figure 1 shows the key parts of the amplifier design.

V. INITIAL RESULTS

The power performance of the device was measured at 150MHz and found to be in excess of 2kW (figure 2).

Following this exciting result, Roke conducted some market research into other applications and markets where this type of amplifier might be of value. Our research showed that the main exploitation routes were in the Medical, High Energy Physics, and EW areas. Further discussions with stakeholders showed that for our amplifier to be suitable, a higher duty cycle would be required. Indeed most potential customers required CW operation! Having assessed the market we decided to concentrate on improving the duty cycle.

For solid state devices a major contributing factor to the degradation of their performance with longer pulse lengths and higher duty cycles is the heat generated in the device. With Si MOSFETs the "on-resistance" of the device increases with temperature, and so in a worst case scenario, this leads to thermal runaway and eventual device destruction. The Junction Temperature is defined as the highest temperature of the actual semiconductor and can be significantly higher than the temperature of the exterior of the device packaging. The maximum junction temperature can range from below 100° to over 200°C depending on the technology.

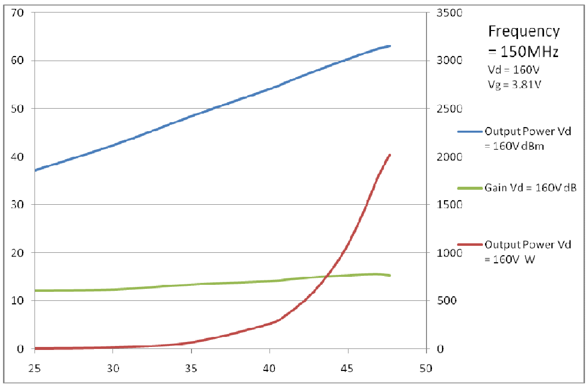

Figure 2. Power sweep measurements for the modified amplifier at 150MHz.

The junction temperature should be kept as low as practically possible by good thermal design practices. The choice of the device packaging plays a major role in this. In short pulse/low duty cycle operation, this is not as important as the device has time to return to ambient temperature during the "off" period. However as the pulse length and/or the duty cycle increase then thermal issues become more critical. It has been demonstrated that solid state technologies suffer degradation in their performance as the pulse length and/or duty cycle is increased [4].

Microsemi provides quite detailed instructions for methods and techniques for mounting their devices in the most thermally efficient manner [5]. In the original implementation of the VHF SSPA the duty cycle was considered to be so low that we were not concerned with thermal aspects. A thin aluminium baseplate was used in the design but this was mostly to provide mechanical support to the device and PCB. We decided to make better use of this baseplate and conducted some thermal analysis using a commercially available solver. We decided on thickening the baseplate and changing the material to copper. This combined with an application of thermal grease between the device and the baseplate would help to remove the unwanted heat. The next issue to address was having moved the heat from the device, where would we dissipate it? The answer lay in a heatsink with forced air cooling.

The temperature of the baseplate was monitored close to the where the device was mounted using a thermocouple. We also increased the charge storage of the test system by increasing the storage capacitance. This also required

VI. FINAL RESULTS

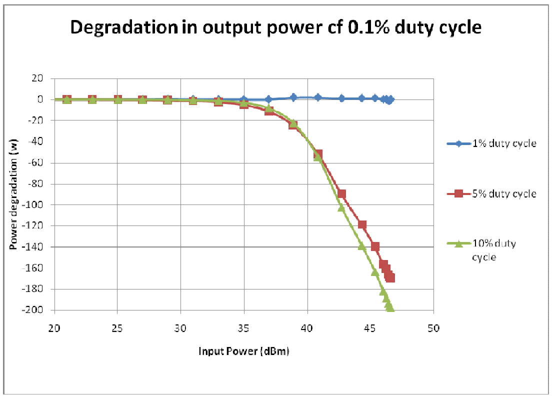

Figure 3. Degredation in output power when compared to the original 0.1% duty cycle result.

modification to the charging circuit to keep the RC time constant to a reasonable value.

Measurements were made for various duty cycles and various pulse lengths. It was found that the maximum duty cycle that could be realistically achieved was 10% representing a hundredfold increase in the duty cycle over the earlier reported results. The average output power in the pulse was measured as a function of input power. The measurements were referenced to the output power for the SSPA when operated at 0.1% duty cycle. The pulse length (i.e. "on" time) was kept at 340us for all measurements.

The figure 3 shows that for 1% duty cycle the performance is the same as for the 0.1% duty cycle case. However as the duty cycle is increased the output power degrades.

The baseplate temperature measurement remained constant during these measurements, indicating that the drop in performance was not due to thermal issues. If the drop in performance at high duty cycles was not due to thermal issues, then it was probably due to power supply issues. The drain supply was monitored on the SSPA board by means of a high voltage probe and a Digital Phosphor Oscilloscope (DPO). This showed that during the "on" pulse the drain voltage could droop quite dramatically (of the order of 30V), despite the addition of extra capacitance. Such modulation of the drain supply would have an adverse effect on the performance of the device. This demonstrates the need for active monitoring and deliberate modulation of the drain supply (such as is employed by Nujira with their patented HAT™ technology [6]).

VII. TESTING HV ELECTRONICS

In an age where digital electronics and low battery voltages dominate the RF and Microwave community, the art of testing HV electronics seems to have become the preserve of the electricity supply and distribution industry. Valve amplifiers with their high voltage anode and grid supplies are a rare exception. Even the tube in your living room is rapidly becoming a thing of the past.

However as shown in this paper HV semiconductors do exist, and when testing them the safety implications need to be taken into consideration. "Volts jolt but current kills" is an oft quoted simplification, but more correctly it is the total energy discharged through a person that is arguably the most important consideration. The most obvious place for storage of energy in a HV circuit is in the capacitors, but also remember that tracks on PCBs, supply cables (especially co-ax) and even inductors can store significant charge.

It is generally accepted that 3J of energy stored in a capacitor is sufficient to kill if the current path passes through the heart, and that an energy level of 10J any discharge path will result in an almost certain fatality. If we take a 'factor of ten' precautionary approach that stored charge greater than 0.3J is to be treated as potentially dangerous, then we can calculate that at 1kV, the total capacitance in an experiment should not be allowed to exceed 1µF!

VIII. S.I.D.E.

When working with HV electronics, the principles of S.I.D.E. offer a good form of defence;

Switch off i.e. remove the source of mains power from the experiment
Isolate i.e. provide a suitable air gap in power supply chain
Discharge i.e. bleed any residual hazardous stored energy to earth
Earth i.e. clamp the experiment to earth

How this is realised can be scaleable with the size and potential risk of the experiment from simple interlocked boxes to major facilities such as Roke's High Voltage Test Facility (HVTF) [7].

The VHF SSPA described above was tested using an interlocked safety box. The box was rated to withstand energies of up to 1J. The lid incorporated DPDT switches which connected the device and storage capacitors to the power supply when the lid was closed, and connected the device and the storage capacitors to earth through dump resistors when the lid was opened. Key elements of this design included multiple switches in an attempt to prevent "user intervention" and redundancy in discharging circuits and warning signals in case of component failure.

At the other end of the scale are test facilities such as the HVTF. This facility consists of two screened chambers and a separate control office. The screened chambers act as Faraday Cages around the experiment and measurement equipment to prevent any leakage of the electric field. They also act as physical barriers. The principle of operation is that the experiment is contained within the main High Voltage Chamber (HVC). The second Test Equipment

Figure 4. HVTF – High Voltage Chamber.

Chamber (TEC) contains the measurement equipment, which is galvanically isolated from the actual experiment, which in turn is isolated from the control office where the experiment is controlled and monitored. No mains voltage is able to be present in the HVC when the doors are open, by means of a pneumatically operated isolation switch. This covers the first two requirements for S.I.D.E.

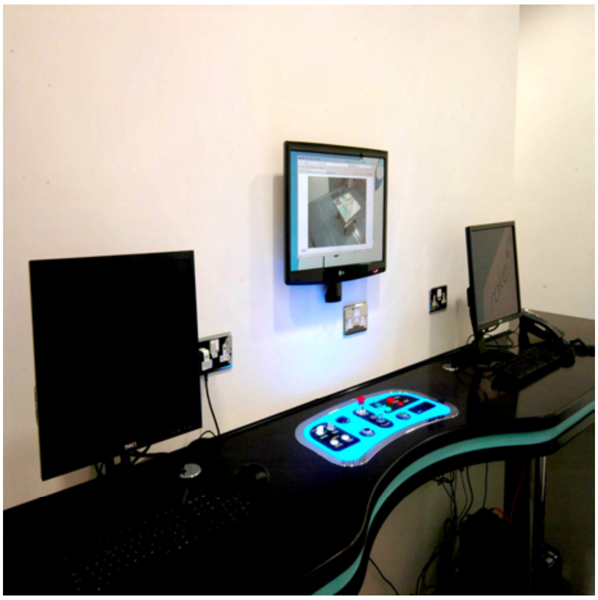

Figure 5. HVTF – Control Office.

Discharge and Earthing can be achieved with the aid of discharge and earth sticks, but this is heavily discouraged, and we place a requirement on the designers of each experiment that they include at the very least automatic discharge of the experiment once the supply voltage is removed. Automatic earthing is harder to achieve but we ensure that all exposed metal that could conceivably store an induced charge are earthed. This includes any object left in the HVC, even if not directly connected with the experiment (e.g. gantries and step ladders).

IX. CONCLUSION

The design of a HV SSPA has been described. The HV SSPA uses low cost Si MOSFET device to deliver over 2kW of pulsed power at 150MHz. Work to extend the capabilities of the SSPA to higher duty cycle operation has been reported. Further we have discussed methods of safely testing HV electronics.

REFERENCES

[1] Mike Kossor; A Broadband HF Amplifier Using Low-Cost Power MOSFETs; QST Magazine; March and April 1999.

[2] ARF475FL Datasheet

[3] Richard Frey; ARF475FL 128 MHz Linear Pulse Amplifier; Application Note APT06010

[4] M. Walden, “Pulsed Power Operation of Commercially Available Silicon Carbide MESFETs” Proc. GAAS 2001 – The European Gallium Arsenide and related III-V Compounds Application Symposium, September 2001, London, UK

[5] G Krausse, D Frey, G Choi; DRF Device Mounting Procedures and Power Dissipation; Application Note 1810

[6] http://www.nujira.com

[7] http://www.roke.co.uk/20091029469/press-releases/roke-launches-world-first-in-high-voltage-testing.html