

Design Challenges in HBT MMIC Amplifier Bias Circuits

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ABSTRACT

During the development of a custom HBT MMIC, solutions will be evolved for the RF and DC circuits in parallel with the packaging and thermal design. The type of MMIC being developed will determine the relative difficulty these areas present. Following a brief introduction to HBT MMICs, this paper focuses on the issues associated with the design of the DC bias circuit, which need to be correctly addressed if the full performance capability of the process is to be unlocked. Merits and disadvantages of basic and advanced bias schemes are discussed for circuits targeting Class A through to Class AB operation.

INTRODUCTION

Hetero-junction Bipolar Transistor (HBT) Monolithic Microwave Integrated Circuit (MMIC) technology is firmly established and has been serving the RF & Microwave industry for many years.

Simplistically, the technology can be considered as a means to integrate bipolar transistors, diodes, resistors, capacitors and inductors together on a single integrated circuit. A typical MMIC is shown in Figure 1 below.



Figure 1: A plastic packaged MMIC (lid removed), with support components, on an FR4 PCB.

The high useful operating frequency (GHz) and high operating current density ($200\mu\text{A}/\mu\text{m}^2$) features of the technology make it eminently suitable for realising a vast range of different products from low power multifunctional circuits through to power amplifiers. From a designer's point of view, an important fact which distinguishes GaAs HBTs from traditional Silicon bipolar transistors, is that the 'V_{be}' of these devices is somewhat higher at around 1.3V, and is subject to a negative temperature slope giving a variation of around $\pm 0.1\text{V}$ over typical operating

temperature ranges. Other than this, from an initial design perspective, HBTs can be thought of simply as very fast, high performance bipolar transistors.

Finally, it is worth noting here, that standard processes only support NPN devices, which we will see is a major limitation in the scope of bias circuit design that is possible.

APPLICATION CHALLENGES

Any HBT MMIC development requires consideration of at least the following elements:

- Circuit design
 - High frequency electrical circuit
 - DC electrical circuit
 - Thermal circuit (ie modelling effects of device self heating)
- Packaging and assembly design
 - Electrical performance
 - Thermal performance

Design can be relatively straightforward for cases where there is good headroom on the supply rail, only modest RF powers are required, and the circuit is allowed to operate largely as a Class A design. Here, the design areas listed above are relatively independent, and the development can generally be undertaken using a simple bias scheme, and basing the RF design on standard foundry s-parameter data, which if representative should almost guarantee 1st pass design success.

The other extreme is the case where there is minimal headroom on the supply rail, and considerable RF power is required from devices, necessitating operation nearer to Class B to achieve combined efficiency and linearity targets. In this case, the RF, DC and thermal circuits become highly interactive, and circuit design becomes a potentially more iterative process as the design areas listed above become significantly more interdependent.

One important means to limit this unwanted interaction, to enable design to be undertaken in a more deterministic and less iterative manner, is by appropriate development of the DC base bias circuit topology.

For the purposes of this discussion, we will say that the most demanding case we will consider is the development of a bias circuit for an HBT MMIC for use in a battery powered equipment such as a mobile phone,

required to run from an unregulated DC supply in the 3-4V region. Also, we would like to consider design options for both low power Class A circuits through to high power Class AB circuits.

Starting from the HBT shown in Figure 2 below, we will develop basic base bias circuits, to highlight areas which present a particular design challenge. Means to mitigate these challenges will be proposed, and the merits and disadvantages discussed.

This paper will conclude by showing how this design knowledge can be used to develop alternative high performance bias circuits, by using one of the authors patent pending designs as an example.



Figure 2: HBT Transistor to bias

BASIC BIAS CIRCUIT DESIGN

The addition of a few components to the transistor of Figure 2, takes us to one of the simplest forms of bias circuit possible shown in Figure 3 below.

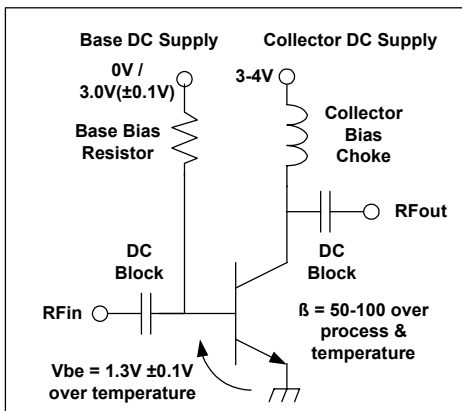


Figure 3: A simple HBT bias circuit

In this case, the collector bias remains permanently connected through the bias choke, and the circuit is activated by a switched regulated DC voltage fed to the base via a resistor, which also functions as an RF block to some degree, additional series inductance being added to improve this if required. Leakage current in HBTs is very low, and so permanent collector bias works for most battery powered applications. Whilst the base current injected will remain fairly independent of temperature and the modest supply rail variations shown, this circuit suffers from a number of problems. Beta variation with process and temperature causes the

collector current to vary, in turn causing poor RF and DC performance. Secondly, if the transistor was a large 'power' device, the current required from the base supply may be of the order of tens of milliamps, which does not lend itself to connection to a low power Silicon IC control circuit as may be typically used. Finally, this sort of topology will not operate well as a so-called deep Class AB power amplifier, this class being required for a good efficiency/linearity trade off in a mobile phone transmit power amplifier (more on this shortly).

Two approaches could be considered here for reducing the circuit's sensitivity to process, temperature and supply rail. The classic approach of the addition of an emitter degeneration resistor would yield a serviceable topology for very low power operation, as would the use of a current mirror, which works very well in an IC environment. These approaches are shown in Figure 4 and Figure 5 respectively.

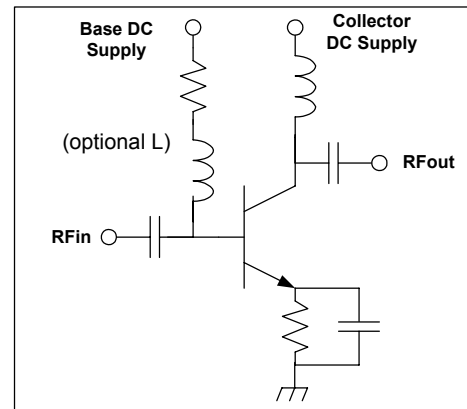


Figure 4: Bias Stabilisation by emitter de-generation

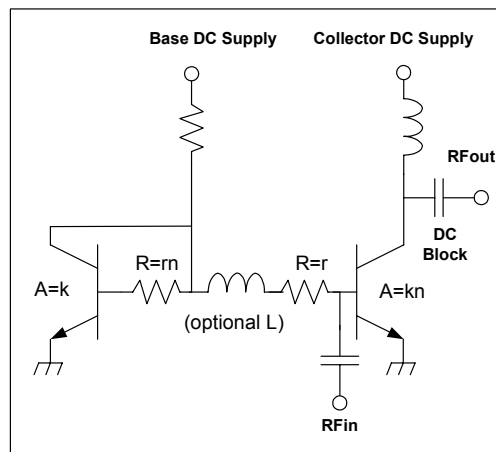


Figure 5: Bias stabilisation by current mirror

However, we are interested in a developing a solution capable of use with power amplifiers too. So for this case, the next stage is to add DC buffering in the base bias feed. This is typically achieved by use of an emitter follower from the control line as shown in Figure 6. This improved circuit reduces the potentially high current demand from the regulated control line to an acceptable level by transferring most of the drain to the unregulated supply.

This circuit however has a new disadvantage over the original circuit of Figure 3, in that we have run out of voltage headroom on our control line and our circuit is now critically sensitive to temperature and supply rail variation, since we are relying on generating a current source from a potential difference which may vary in this example from 0.1V to 0.7V across the bias resistor.

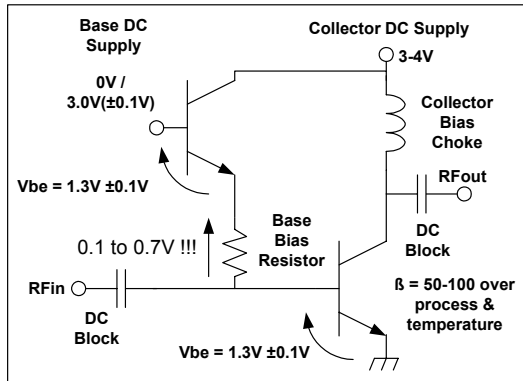


Figure 6: HBT bias circuit with DC buffer

A variation factor of the order of seven is unacceptable, and some temperature and power rail compensation is required. The addition of two diodes and a resistor yields the circuit of Figure 8. This circuit relies on good thermal coupling such that the diode voltage tracks V_{be} changes with temperature, clamping the base voltage at the emitter follower, reducing the circuit's sensitivity.

Before we leave the circuit of Figure 6, another important advantage needs to be described. The addition of the emitter follower transistor means that we now have a circuit which can be tailored to provide a Class AB mode of operation. Class AB amplifier design is a subject in itself, so only a basic description is necessary here, to highlight features of a bias circuit that are needed to address this requirement:

An aside: Class AB operation basics

In Class AB, the circuit is set up so that in the absence of an RF signal, the main transistor is biased at some low quiescent collector current, such that for low RF drive levels it functions as a linear amplifier. As the RF drive level increases, rectification causes the circuit to self-bias, and operation is more towards Class B. This can be explained with reference to Figure 7 below.

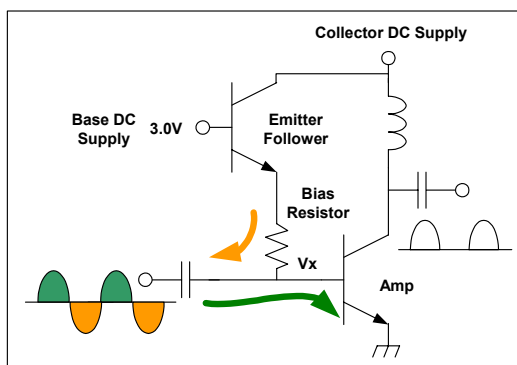


Figure 7: Class AB operation

On the forward current half cycle, V_x tends to rise slightly as the RF current drives the base of the main transistor. This clamps the base emitter voltage of the emitter follower, such that it does not supply current to the main transistor. On the negative going half cycle, V_x drops, and the 'return' RF current is supplied from the emitter follower. The rectification which occurs means the time averaged voltage at the base of the main transistor is lower than when the RF signal was absent, and its collector current is higher. In this way the circuit operates as a deep Class AB design, and can maintain a much improved total battery efficiency over a wide range of operating powers, than could be achieved for Class A. It can readily be appreciated that the choice of bias resistor will strongly influence the self biasing profile achieved, and indeed there is an optimum value for this component for different modulation schemes and linearity requirements. In practice of course, additional challenges present themselves for good overall Class AB circuit design. However for the purposes of this bias circuit discussion, the need to incorporate features to allow and tailor self biasing has been explained.

To summarise then, the circuit of Figure 6, has reduced control current requirements, and an option for Class AB operation.

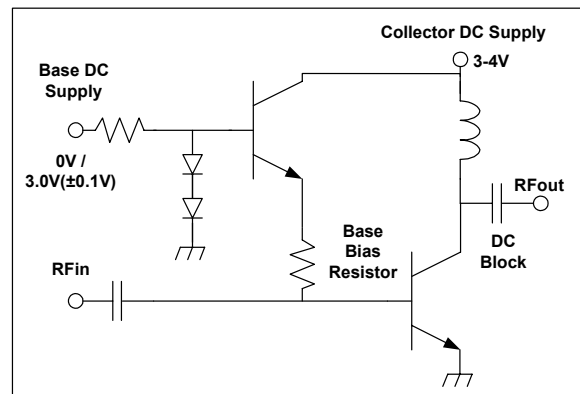


Figure 8: A circuit just suitable for providing deep Class AB bias for a 'saturated' modulation type PA.

The circuit of Figure 8, with the previously described compensation diodes, is our first fully practical bias circuit, minor variants of which may be found for example in deep Class AB GSM HBT power amplifiers MMICs selling in high volume.

However, this circuit is not without its disadvantages. Whilst providing some thermal compensation, the bias point may still vary by as much as a factor of three over a typical temperature range of -25°C to $+80^{\circ}\text{C}$. The control current is rather high again (up to 15mA in some cases), due to the need to waste a certain amount in the diode clamp. Next, whilst suitable for driving a power amplifier in a Class AB mode for the case where a saturated modulation scheme is used, it is not suitable for use with linear modulation schemes (CDMA etc), where unacceptable adjacent channel leakage would result for adequately low quiescent currents. Finally,

limitations in device models and CAD software, means this sort of circuit is difficult to design for 1st pass success, and iterations of many variants may be needed to find the one that gives the best trade off between performance and yield. It is essential, for mobile phone power amplifiers in particular to optimise every last bit of performance from the smallest die possible, since only the very best components will sell successfully.

From Figure 8, to take the next step in bias circuit development to achieve a circuit that works well with linear modulation and lower control currents, takes us to the area of advanced bias circuit design, where many patent applications can be found. This level of IP generation highlights the importance of a good bias circuit - it really is a major key to unlocking the performance of the target HBT process, for the application in hand.

Reading through these works reveals a surprising range of clearly distinct methods used to tackle the problem. On one extreme, solutions exist that use relatively simple circuits combining the three basic forms of biasing we have discussed (resistive based, current mirror based & emitter follower based). The topology is configured to access the benefits of each yielding a circuit that works well for high power linear modulation Class AB amplifiers. On the other extreme, solutions can be found which are based on more complex circuits using multiple current mirrors or a control loop approach. Whilst more complex in terms of the number of components, these solutions are still adequately compact on-chip. Finally, to augment these schemes, modifications to the standard HBT process are occasionally made. Such modifications include special ultra-compact low frequency transistors for the bias circuit, or changes to the metalisation arrangements for better thermal performance.

Before such an advanced bias scheme is discussed, it is appropriate to summarise the key points of the discussion so far:

Why is proper design of the bias circuit topology so important?

- To unlock the full performance potential of the HBT process
- To improve the ‘designability’ of the circuit to reduce development costs

What are the design issues?

- Need to optimise the bias circuit interaction with the RF signal
- Need a power down function
- May need high power / low power modes & linear / saturated modes
- Need minimum current draw from regulated control lines.
- Need good process, supply and temperature tolerance
- Need a compact on-chip implementation

Why are these issues difficult?

- Some solutions require large on-chip components such as inductors to maintain linearity, and so reduce the cost effectiveness of the design.
- A switched 0/2.8V ‘enable’ control line is typically available. NPN devices only, means that it is difficult to design a topology with a power down mode, with low control current draw in the on-state.
- A bias circuit with different modes is difficult to design without compromising some aspect of performance.
- Emerging high performance processes offering a ‘ β ’ circa three times higher than conventional HBT will mean suppliers using conventional technology and simple bias circuits only could eventually be forced from the market.
- High $V_{be}=1.3V$, compared to supply rail typically 3.0V makes useful circuits involving stacked devices impossible.
- High V_{be} in combination with low V_{cc} and typical temperature coefficients, can lead to poor stability over temperature.

ADVANCED BIAS CIRCUIT DESIGN

The previous section developed simple bias topologies by sequentially adding components until the required functionality was achieved, and then adding further components to correct additional problems that arose along the way.

The understanding that this process has provided, as summarised in the bullet points above, is a necessary precursor to enable more advanced topologies as used in the industry, to be designed.

As an example, the development of one such bias circuit as undertaken by the author will now be discussed. The aim was to generate a bias circuit that could be configured either for Class A operation or for deep Class AB operation and allow for ready modification to include additional features such as switched bias points. Also, and very importantly, to reduce the circuit’s sensitivity to process, temperature and supply rail variation not only in final hardware, but also at the design stage, such that the circuit could be simulated using existing CAD software and models with improved correlation to measurement.

As an R&D consultant to the MMIC industry, ownership of such a circuit by the RFICs Group at Roke Manor Research Limited was clearly highly desirable.

Figure 9 below contains the elements which were asserted to be essential for the aims targeted. The main RF transistor (bottom right) is permanently connected via the collector circuit to the supply rail which may vary from 3.0V at the end of the batteries life up to 6.0V when on-charge. An emitter follower is essential to minimise the current drawn from the regulated control line, which is now shown as the more typical 0/2.8V. A small mirror transistor, in close thermal coupling to the

main transistor, provides accurate monitoring of the quiescent condition in the transistor. From this start point, additional circuitry is required to somehow convert the low level 'sensed' current in the mirror transistor into an 'error' current that can be used to pull the emitter follower's base node down, such that the circuit reaches the desired equilibrium.

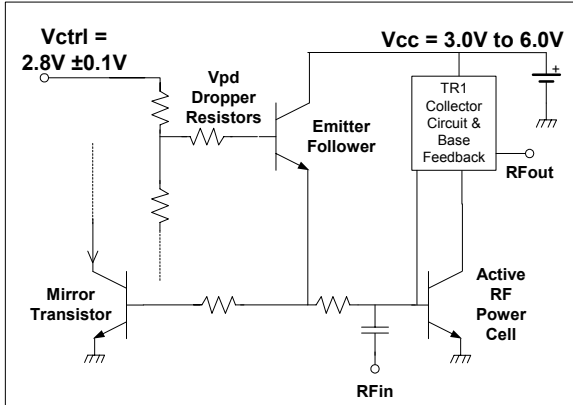


Figure 9: Essential Elements for the example advanced bias circuit discussion

As may be anticipated, the topology is beginning to look like one of the "control circuit" types mentioned earlier, one missing element clearly being a reference signal of some sort. The desired control loop concept in this case is summarised in Figure 10 below.

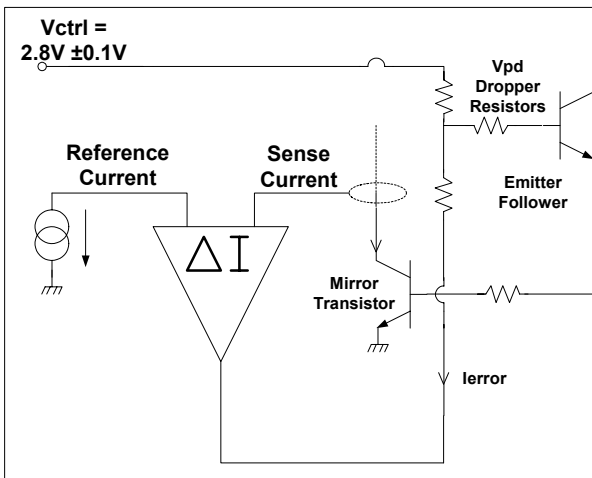


Figure 10: Control Circuit Concept

A reference current generator can readily be designed using another emitter follower as shown in Figure 11 below. This sets up a reference current in the collector, determined by a single resistor in the emitter arm to ground. The temperature coefficient of this resistor can often be made equal and opposite to that of V_{be} , such that the current produced is independent of temperature and varies only with the regulation of the V_{pd} line.

Addition of equal resistors in the collector arm of this transistor, and the original mirror transistor, converts these sense and reference currents into voltages. Providing we can find a way to perform a relative comparison between these levels, then we have a nice

circuit which aside from the initial reference current generation relies wholly on component ratios. Also, it will be appreciated that the circuit offers good immunity to supply rail variation, since any such variation causes near equal change in both sense and reference voltages.

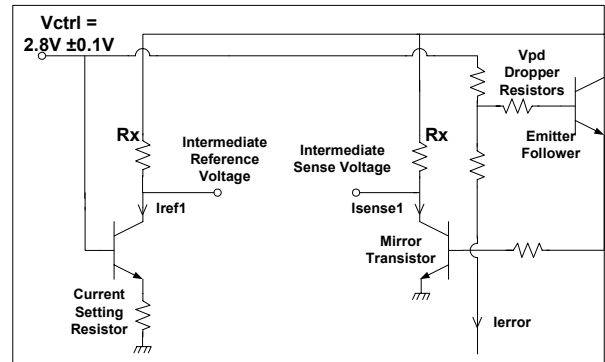


Figure 11: Addition of a reference current generator

The relative comparison and conversion to an error signal was the most difficult problem to overcome, although as often seems the case with circuit topology development, the solution actually appears quite simple. The function is achieved using a current mirror and one further transistor to provide a V_{be} reference and DC amplification of the error. The loop is then closed, as shown in Figure 12 below.

The final stage is to add a power down switch and additional diode to block a leakage path. This complete circuit is shown in Figure 13 below. Despite the apparent large quantity of components, this implementation is very compact on chip, since most of the additional transistors are near to minimum size for process, and most of the resistors can be made very narrow and short. Such resistors are more prone to manufacturing spread, but since the circuit primarily depends on ratios rather than absolute values, this can be well tolerated.

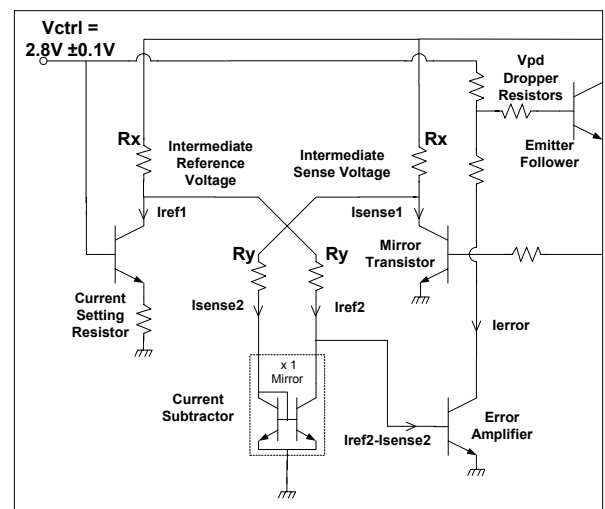


Figure 12: Addition of the differential current comparator and error amplifier.

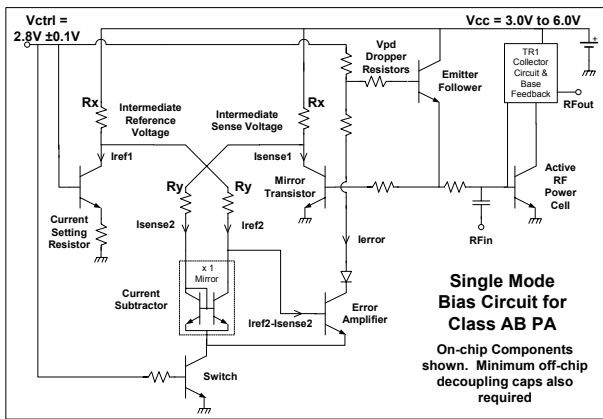


Figure 13: Essentially complete circuit, providing bias for Class AB Power Amplification.

All bias circuits tend to have some natural thermal slope, which causes a drift in quiescent bias level in one direction with temperature. Generally, a positive slope is desired to help achieve the same RF output power at higher temperature. The natural slope of this circuit is in the correct direction, and can actually be tailored as required. It was also found that parameters such as adjacent channel power ratio and 3rd order intercept can be optimised with minimal impact on other circuit parameters, which is an extremely useful feature. Finally to note that additional modifications are possible to realise switched quiescent points, such as would be required for a dual mode amplifier required to operate with either linear or saturated modulation schemes.

Altogether then, this circuit addressed and overcame all of the key issues, and with minimum additional capacitors off-chip can be made to work nicely as a bias solution for linear Class AB amplifiers.

To remove the self biasing feature, a single capacitor can be added across the base emitter junction of the emitter follower. This serves to make the emitter follower a near open circuit to RF, and very linear amplification in Class A results.

Overall this topology proved to be a great success, the features and benefits being summarised as follows:

- Configurability for deep Class AB through to Class A. All configurations maximise RF performance, especially linearity.
- Power down and other modes can be supported.
- Ultra low current draw from control lines, typically 80% lower than other industry solutions
- Excellent process, supply and temperature tolerance – by design.
- Excellent ‘designability’ – single component changes largely affect one design parameter only.
- Compact on-chip inductorless implementation
- Inherently designed for high manufacturing yield on any HBT process.
- Excellent process transportability

SUMMARY

The importance of good bias circuit design for HBT MMICs has been explained, and the key issues that need to be considered have been made clear, through examples of simple circuits. This basic knowledge primer is necessary for anyone wishing to design a more advanced topology.

One such topology is the author’s patent pending configurable bias circuit, and by way of example its development has been described. This circuit was shown to address the key issues raised, and can be configured for either Class A or deep Class AB. In all configurations the circuit offers very low process, temperature and supply rail sensitivity, giving improved yield in final hardware, and improved ‘designability’ at the development stage, enabling 1st pass design success for challenging design specifications to be more readily achieved, than would be possible with more primitive designs.

REFERENCES

This paper refers to circuit and techniques as described in the patent applications: GB0304053, GB0306405, PCT/GB03/01167, & PCT/GB03/01309.

CAUTIONARY NOTE

It must be mentioned that anyone planning to release an HBT MMIC product, would be well advised to conduct a thorough patent search in advance for aspects of the design, such as bias circuit topology.

FURTHER INFORMATION

The reader is invited to visit our website at <http://www.roke.co.uk> for further information on HBT Bias Circuits, and general MMIC and RF ASIC activities at Roke Manor. In particular, the following datasheets can be downloaded:

- http://www.roke.co.uk/download/datasheets/hbt_mmic_design.pdf
- http://www.roke.co.uk/download/datasheets/hbt_bias_circuit.pdf
- http://www.roke.co.uk/download/datasheets/mmic_design_consultancy.pdf

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