

# Easing the Testing Bottleneck in Handset Power Amplifier Development

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**Abstract – This paper describes a test suite that has been developed at Roke Manor Research Ltd to decrease the time required to characterise a power amplifier (PA) design. Current trends of increased performance to meet new standards and the commercial pressure of time to market has meant that power amplifier design cycles need to be reduced. These cycles require modelling, design, implementation and then test. Testing has long been a bottleneck in the iterative process, and this will only get worse as testing requirements increase. Roke has invested considerable effort in developing a highly automated and configurable test facility for the dedicated purpose of testing handset PA devices. This paper aims to demonstrate some of the steps that can be taken to improve the efficiency of the testing process.**

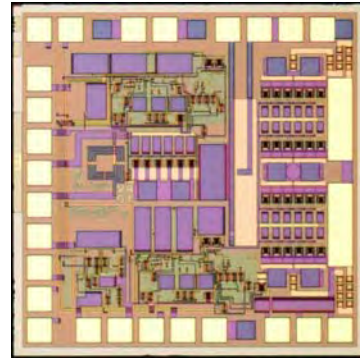
## I. INTRODUCTION

The design of Power Amplifiers for mobile devices is a challenging task. Onerous electrical design targets will be specified - for example, power output, operating bandwidth, efficiency and linearity. The increasing demand for wireless bandwidth has meant that the controlling standardisation (ETSI, 3GPP) has tightened these design targets.

The final PA 'solution' must be squeezed into a module perhaps 3mm by 3mm in size. Ideally a single 'chip' solution is required, although at the time of writing, a handful of 0201 size components are typically also squeezed into the module, for power matching and bias feeds. The sheer compactness of the design makes exact modelling of the device a near impossibility, even with state of the art EDA packages. The components, tracks and bond-wires within the module are highly interactive, and a minor change to one feature or component typically impacts on all three key electrical parameters (linearity, efficiency, power output).

It will be appreciated that the development of such a product is a highly iterative process. To add to this, fierce market competition means design cycles are short, and design targets may

change during development, if market 'intelligence' suggests a change is required.



**A Power Amplifier Die Designed at Roke**

Roke has designed Power Amplifiers & Power Amplifier Modules for many commercial customers including designs for GSM, through to WCDMA.

To reduce our design cycle time per iteration of the product, an integrated design & test strategy has been adopted. Our aim has been to devise a test system where, at the press of a button, a PA module can be completely analysed, with results output into Excel and back into our EDA tool for deltas to be examined. The testing process has also been optimised to take as short a time as possible.

This paper largely describes the automated test process we have developed, and its interaction with the EDA tools. Firstly, the testing aims must be determined. The paper then looks at the setup and configuration of a test bench before devising an appropriate test schedule.

## II. TESTING AIMS

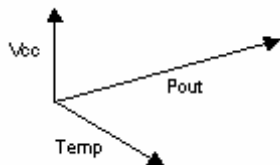
Typically performance parameters are driven by the requirement for a module to be integrated into a design that conforms to a particular standard (such as ETSI or 3GPP). Common specification parameters for PA devices are output power, efficiency, Adjacent Channel Leakage Ratio (ACLR) etc.

Whilst improvements are always being made in terms of simulation, the highly non-linear and integrated nature of PAs means that a multi-iteration development cycle is inevitable, and that the testing process within this cycle will use important development time. Any improvements in the testing process are therefore attractive to the PA designer.

It is important when configuring a test bench to distinguish between testing for the purpose of design development or testing for the purpose of proving conformity. The differences are subtle.

Testing for conformity is driven by the specifications for which the performance of the device must meet (NB PA performance parameters must be extracted from full radio level plan). Conformity testing of a PA will typically concentrate on a smaller number of operating points crucial to meeting the specification (such as output power and ALCR performance), but these will be tested over a wider range of operating conditions – variation in power supply, temperature etc.

Each operating condition will add an extra dimension to the measurement process and in practice it is impossible to run a device over every condition that may be encountered, thus a test schedule must be generated (this will be examined later).



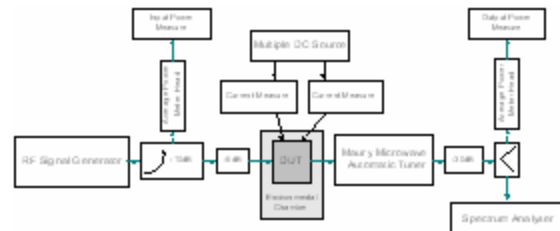
Typically in testing for design, the user may choose one or two operating points for each stimuli e.g. for frequency middle of GSM900/1800 band, default or low voltage settings. This will limit the total number of operating points dramatically. It is likely that for each operating point, a power sweep will be required to determine the non-linear behaviour of the PA.

Obviously, it will be of most benefit to use the same test bench for both testing purposes, as that way the designer can be confident after the design/test phase that the device will match conformity testing.

### III. TEST BENCH

To perform a test on a PA device, first the stimuli (voltage sources, input signal etc) must be applied to the device. Secondly the measurement is then taken. Ideally, a ‘universal’ test bench will be able to apply all of the stimuli necessary to test for design/conformity across the full range of operating conditions, and measure all of the required parameters, without an operator having to make any physical changes to the test bench. This will facilitate the automation of the test process.

A block diagram of a test bench that covers the majority of tests required for a PA is shown below.



**Test Bench Block Diagram**

The PA device is mounted within an environmental chamber. This can set the temperature device overall the full operating range of -55°C to +125°C.

The RF input signal is provided by a signal generator. Typically this will have an arbitrary waveform generator capable of modulating the output frequency with GSM, EDGE, WCDMA etc. The voltage supply is supplied by a DC source.

The variable load is supplied by an automated tuner. At Roke, a Maury tuner is used. This can provide full smith chart coverage from 800MHz to 2.5GHz, and to a VSWR of 20:1. It also exhibits exceptionally low loss, thus can remain in the system for non load pull tests. It should be noted that this is currently a fundamental load pull system.

Power meters are used to measure the input/output power of the signal. In the case of a pulsed signal (such as GSM), a thermal power head will be used to provide a more stable measurement due to its longer time constant.

The DC currents are measured using digital multi-meters or DC probes/oscilloscope for

pulsed signals. Both ACLR and Harmonics can be evaluated using a spectrum analyser.

This test bench cannot currently perform receive band noise or S parameter tests, without physical changes to the test bench setup

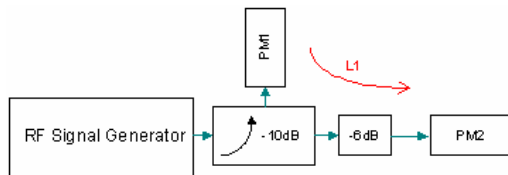


**The Test Bench**

*Calibration*

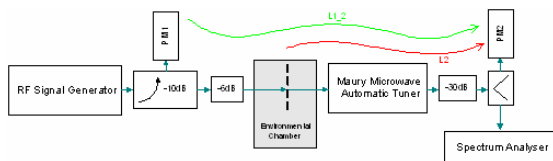
Calibration is required to ensure the input and output power at the DUT is normalised to the readings on the input and output meters (PM1, PM2). Calibration is achieved via the following process:

- 1) Connect PM2 to the DUT input terminal:



$$L1 = PM2 - PM1$$

- 2) Connect the DUT input to DUT output. Return PM2 to its usual position.



$$L2 = PM2 - PM1 - L1$$

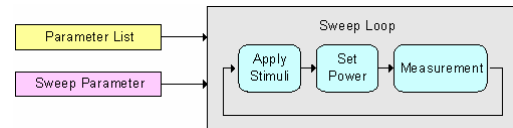
The calibration procedure must be repeated for each frequency point that will be measured as the frequency response of the test bench will not be flat.

*Automation*

It goes without saying that for maximum efficiency, the test bench should be subject to the maximum level of automation possible. All

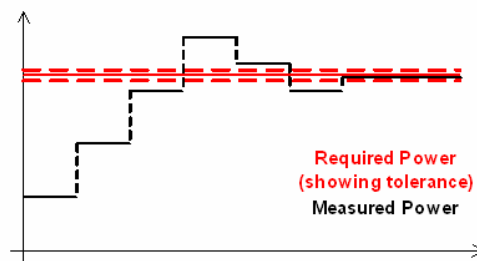
instruments used can be remotely operated by GPIB or RS-232. These are linked to a PC that contains the automation software. Currently the automation software used in either LabView or Maury for load pull testing.

Roke has developed a 'sweep' software utility that is used to control the testing process. The software follows a fixed testing loop (see illustration):



Firstly, the stimuli are applied to the device (the order can be specified). The stimuli are taken from a parameter list that is passed by the calling function, and contains information such as frequency, output power, supply voltage etc. A sweep start/stop/step structure is also passed together with an indicator of which parameter to sweep. This then overrides the parameter list for the swept frequency.

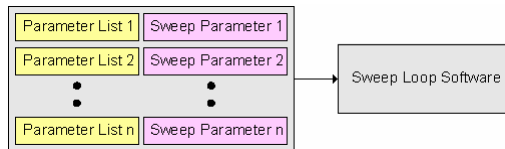
Secondly, the power is set correctly for the device. Closed loop power control is used. For fixed gain amplifiers (e.g. WCDMA), the input power is adjusted. For variable gain amplifiers (e.g. GSM), the input power is first set, then a control voltage is used to set the output power. In both cases, a reducing delta power loop is used to minimise the time it takes to arrive at the correct power settings. This involves halving the power jump step until the power is set to the specified tolerance (see illustration). Efficiency is improved further by choosing consecutive operating points that require only a small change in power.



Finally, the specified measurements are taken by the various items of test equipment – input/output power, ACLR, harmonics, DC current etc. The data is then tabulated and saved into an Excel spreadsheet.

For any testing purpose, it is likely that a number of sweeps of different parameters will be required. Roke has also developed a higher

level scheduler program that can call up a number of different sweeps consecutively.



This level of automation means that a complex set of tests can be left to run for a long period of time (possibly up to several hours) minimising the human contact required.

Current the test bench can only sweep in one dimension. It is intended to add multi-dimensional sweeps at a further date. An additional piece of software is currently used to repeatedly call up the scheduler software to run identical sweeps, but changing the temperature.

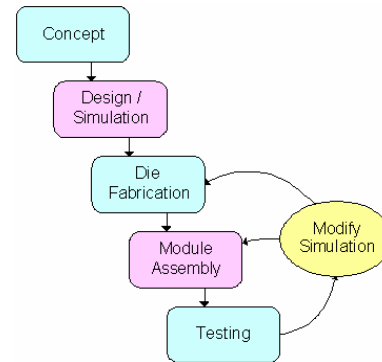
#### IV. A TEST SCHEDULE

To efficiently minimise the amount of testing required, a test schedule must be devised that utilises the lowest number of measurements.

When testing for conformity, there will be a mandatory list of measurements that must be completed for the conformity to be determined. However, the test schedule can be arranged to minimise the time taken for each measurement:

- All measurements are conducted together for each operating point
- In changing between operating points, the slowest state changes are (starting with slowest) – temperature, load pull, power. So for example all tests should be conducted at one temperature before moving to the next temperature.

In testing for development, the same broad coverage of testing for conformity is not required. Instead, more detailed testing is likely to be executed around chosen operating points that are likely to match those in the simulation, in order to provide feedback for the design iteration process.



There are many options for selecting an appropriate test schedule, some examples are:

- Selectively choose conformity tests around known design operating points in simulation
- Add more detailed tests around operating points (e.g. around amplifier saturation)
- Information that is too power hungry for simulation – e.g. ACLR over load pull.

The result is that by choosing an efficiency test schedule, the development time is reduced. Coupled with the automation level provided by the test bench, and the user has a true ‘press and go’ test facility. The result is a better chance of catching subtle changes to performance with design modifications.

#### V. RESULTS FEEDBACK

Ideally the test schedule will be harmonised with the simulation tool. For example, for our PA device we might have set operating points at set simulation frequencies, powers etc.

The current test bench software allows results to be fed back into the EDA tool. This means that a direct comparison between predicted performance and real test data is possible. From this, the designer is able to improve the modelling of the PA schematic.

Some example results plots are show below and the end of this paper.

Ultimately, the designer is able to test the PA for conformity against the production specifications. The automated nature of the bench means that this process is achieved quickly and with little effort, and thus a large number of devices can be evaluated. This is particularly useful for example when supplying a customer for a sample run.

In terms of results generation, the test bench can also be used efficiently as a benchmarking utility, to evaluate third party devices for use in a mobile handset. This application has already been successfully used for one customer providing tens of thousands of measurement points over only a few weeks of testing.

## VI. CONCLUSION

In this paper, ideas have been presented to improve the efficiency of the testing process based on PA design. It has been argued that a combination of increasing performance demands, and size reduction have meant that an iterative design process is required, and that testing is obviously required in each stage of

the process. It has been demonstrated that at Roke, a testing facility and processes have been developed that provide fast, highly automated and highly configurable performance feedback on the device.

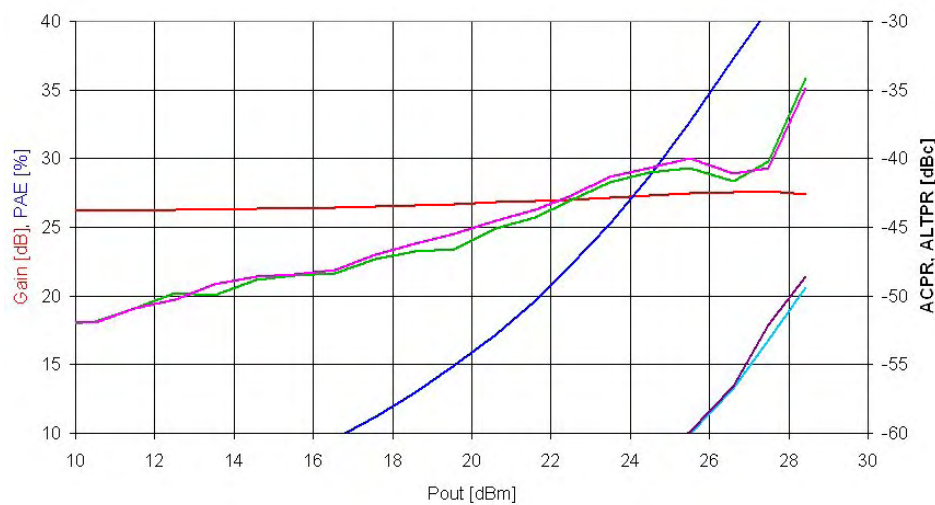
## VII. ACKNOWLEDGEMENTS

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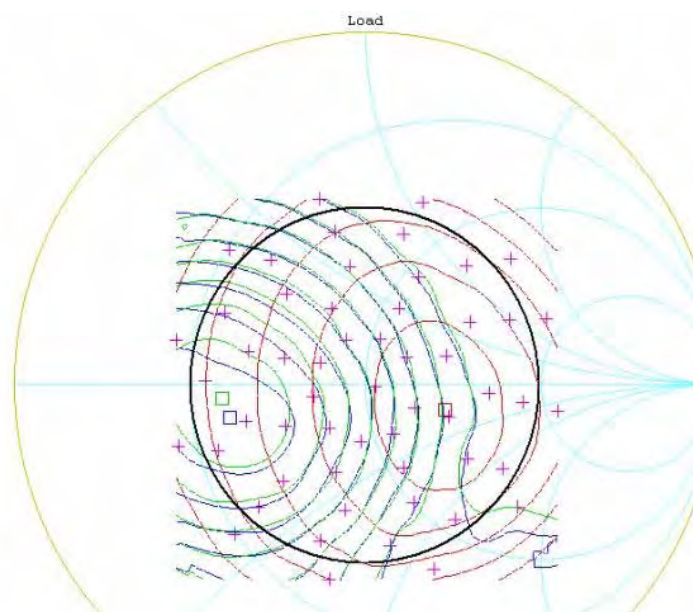
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## Gain, Efficiency and ACLR against Output Power

```
Fixed Load Pull
Freq = 1.9488 GHz

Eff      max = 42.75 %
at 0.2425<-18.32
5 contours, 4.00 % step
(24.00 to 40.00 %)
acp_adj_up min = -49.75 dBc
at 0.3965<-165.68
8 contours, 3.00 dBc step
(-48.00 to -27.00 dBc)
acp_adj_lo min = -50.28 dBc
at 0.4084<-173.88
8 contours, 3.00 dBc step
(-48.00 to -27.00 dBc)
Specs: OFF
```



Plot of Efficiency and ACLR against Load Pull